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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,617	01/26/2004	Edward R. Rhoads	ITL.0241D1US (P7376D)	8924

21906 7590 07/31/2006

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,617	RHOADS ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *16-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 26-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/06 &9/27/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Preliminary Amendment

1. This Office action is in responds to the Preliminary Amendment filed on January 26, 2004, claims 16-25 are canceled, claims 1-15 and 26-30 are pending in the application.

Information Disclosure Statement

2. The Information Disclosure Statements filed on 2/25/2004 and 9/27/2004 have been considered.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-15 and 26-30 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,948,099. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the claimed features of he present Application serial No. 10/764,617 are transparently found in U.S. Patent no. 6,948,099. Take an example of independent claim 10 of the present Application and independent claim 2 of the U.S. Patent as following table:

Application Serial No. 10/764,617	U.S. Patent No. 6,948,099
A non-volatile, reprogrammable semiconductor memory comprising:	A memory comprising:
a plurality of addressable partitions, including a partition storing an operating system, and	a first portion storing a primary operation system;
a storing location storing an address for one of said partitions in association with information about the information stored in said partition.	a second portion storing a recovery operating system and instructions adapted to obtain a new operating system from outside said memory; and
	wherein said memory is a FLASH memory.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-15 and 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Tallam (US PAT. 6,948,099).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Tallam discloses a method of organizing stored information on a non-volatile, reprogrammable semiconductor memory (14, figure 1 and col. 2 lines 28-44) comprising partitioning said memory into a plurality of partitions (20 and 22, figure 2 and col. 2 line 66 through col. 3 line 15), each having a defined address (col. 2 line 45 through col. 3 line

15), and storing the defined address for one partition in another partition (col. 2 line 66 through col. Col. 4 line 6).

Regarding claim 2, Tallam discloses the method further including storing information about the number of partitions (col. 4 line 59 through col. 5 line 39).

Regarding claims 3-5, Tallam discloses the method further including storing a boot loader (102, figure 5), a file system (106, figure 5), and a kernel for an operating system (104, figure 5) in one of said partition (col. 4 line 59 through col. 5 line 18).

Regarding claim 6, Tallam discloses the method further including storing information in association with the addresses about whether or not an integrity check needs to be done on the data stored at association address (col. 4 lines 26-50).

Regarding claims 7-9, Tallam discloses the method further including storing, in association with the address of a partition, information about the type of information stored in the partition, and storing information about whether or not the information stored at given partition is a boot loader, a kernel or a file system, and storing information about the load address for said information in association with said address (col. 4 line 59 through col. 5 line 38, figure 5).

Regarding claim 10, Tallam discloses a non-volatile, re-programmable semiconductor memory (14, figure 1 and col. 2 lines 36-44), comprising a plurality of addressable partitions, (20 and 22, figure 14), including a partition storing an operating system, i.e., primary operation system (22, figure 2), a storage location storing an address for one of said partitions in association with information about the information stored in said partition (20, figure 3, and col. 3 line 16 through col. 4 line 25).

Regarding claim 11, Tallam discloses a non-volatile, re-programmable semiconductor memory is a FLASH memory (col. 2 lines 36-44).

Regarding claims 12-25, Tallam discloses a non-volatile, re-programmable semiconductor memory wherein one of the said partitions stores a basic input/output system (32, figure 3), a file system (106, figure 5), a kernel for an operating system (104, figure 5), and a boot loader (102, figure 5).

Regarding claim 26, Tallam discloses a processor-based system (12, figure 6) comprising a processor (65, figure 6), a volatile memory (68, figure 6) coupled to said processor, and a re-programmable, non-volatile semiconductor memory (14 figure 6) coupled to said processor (col. 5 line 43 through col. 6 line 24), the semiconductor memory including a plurality of partitions (20 and 22, figure 2), one of said partitions storing an operating system (22, figure 2), and another of said partitions storing the address of the other partitions in association with information about what is stored in each of the partitions (figure 5 and col. 4 line 59 through col. 5 line 38).

Regarding claim 27, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claims 28-30, the limitations of the claims are rejected as the same reasons set forth in claims 12-25.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-15 and 26-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Bunnell et al. (US Pat. 5,594,903 hereinafter Bunnell).

Regarding claim 1, Bunnell discloses a method of organizing stored information on a non-volatile, re-programmable semiconductor memory, i.e., read only memory, (14, figure 1 and col. 4 lines 41-48) comprising partitioning said memory into a plurality of partitions each having a defined address(62, figure 3 and col. 20 lines 56-60), and storing the defined address for one partition in another partition (col. 7 line 45 through col. 8 line 61).

Regarding claim 2, Bunnell discloses a method further including storing information about the number of partitions (col. 6 line 10 through col. 7 line 26).

Regarding claims 3-5, Bunnell discloses a method further including store a boot loader (68, figure 3 and col. 7 lines 53-65), a file system (col. 8 lines 41-56) and a kernel for an operating system (col. 8 lines 21-40) in one of the said partition.

Regarding claim 7-9, Bunnell discloses a method further including storing, in association with the address of a partition, information about the type of information stored in the partition (figure 3), storing information about whether or not the information stored at a given partition is a boot loader, a kernel or a file system, and storing information about the load address for said information in association with said address (col. 7 line 45 through col. 9 line 52).

Regarding claim 10, Bunnell discloses a non-volatile, re-programmable semiconductor memory, i.e., (ROM) read only memory (40, figure 2) comprising a plurality of addressable partitions (figure 2), including a partition storing an operating system (44', figure 2), and a

storage location storing an address for one of said partitions in association with information about the information stored in said partition (col. 6 line 30 through col. 7 line 40).

Regarding claim 11, Bunnell discloses the memory is a FLASH memory (col. 7 lines 45-52).

Regarding claims 12-15, Bunnell discloses the memory wherein one of said partitions stores a basic input/output system (col. 4 lines 49-65), a file system (col. 8 lines 41-57), a kernel for an operating system (col. 8 lines 21-28), and a boot loader (68, figure 3).

Regarding claim 26, Bunnell discloses a processor-based system (10, figure 1) comprising a processor (12, figure 1), a volatile memory, i.e., RAM (40, figure 2) coupled to processor (figure 1), and a re-programmable, non-volatile semiconductor memory, i.e., (ROM) read only memory (42, figure 2) coupled to said processor (col. 4 line 28-48), said semiconductor memory including a plurality of partitions (42, figure 2 and 62, figure 3), one of said partitions storing an operating system (44', figure 2) and another of said partitions storing the addresses of the other partitions in association with information about what is stored in each of said partitions (col. 6 line 30 through col. 7 line 40).

Regarding claims 27, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claims 28-30, the limitations of the claims are rejected as the same reasons set forth in claim 12-15

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee et al. (US PAT. 5,870,520) discloses flash disaster recovery ROM and utility to reprogram multiple ROMs (abstract).

Lin et al. (US PAT. 6,192,456) discloses method and apparatus for creating formatted file allocation table partitions with a hard drive having a BISO-less controller (col. 3 line 34 through col. 4 line 30).

Tsai et al. (US PAT. 5,974,528) discloses microcomputer with embedded flash memory having on-chip programming capability and method of programming data into the embedded flash memory (abstract).

Robinson et al. (US PAT. 5,544,356) discloses block-erasable nonvolatile semiconductor memory which tracks and stores the total number of write/erase cycles for each block (abstract).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Zhuo H. Li

Patent Examiner
July 12, 2006

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